



深圳市诚芯微科技股份有限公司
SHENZHEN CXW TECHNOLOGY CO., LTD.

CX8806/100V Input,10A Output,Synchronous Step- down Converter

CX8806

100V Input,10A Output, Synchronous Step-down Converter

诚芯微科技

DATA SHEET



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CX8806/100V Input,10A Output,Synchronous Step- down Converter

Description

The CX8806 is a high voltage, synchronous step-down controller operates over a wide range input voltage 9V to 100V.

The CX8806 delivers 10A continuous load current with up to 96% efficiency.

The CX8806 operates with fixed frequency peak current control with built-in compensation eliminates the need for external components. Cycle-by-cycle current limit in high-side MOSFET protects the converter in an overload condition. locking mode of short circuit

The CX8806 exhibits protection features that protect the load from faults like under-voltage, over-current and over-temperature.

Features

- 9V to 100V input voltage range
- 10A continuous output current
- 96% Peak Efficiency
- 600 μ A operating quiescent current
- Peak Current mode control
- 150 kHz Fixed Frequency
- Internal compensation for ease of use
- Up to 91% duty cycle
- 0.8V voltage reference
- 1 μ A shutdown current
- locking mode of short circuit
- MSOP10 package

Applications

- Charger in vehicle
- Battery Chargers
- Power adapter

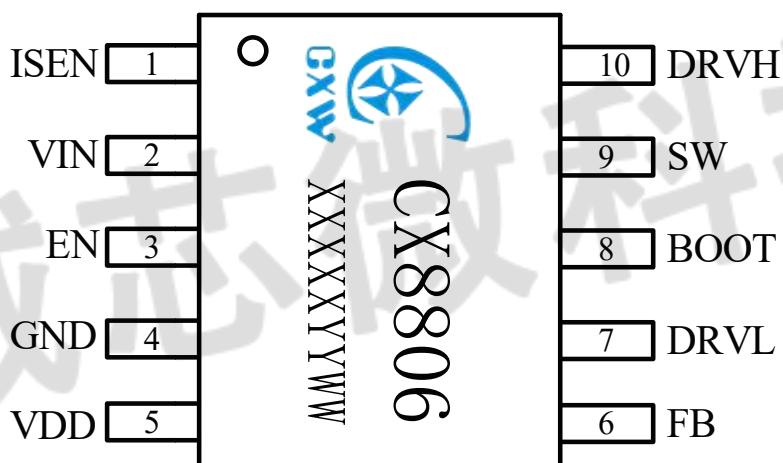
Ordering Information

PART NUMBER	Temperature range	PACKAGE	Number of pins	Wrapping method	Top label
CX8806	-40°C~140°C	MSOP10	10	Tape	CX8806 XXXXXXYYWW

Note:The screen printing batch of the top label (XXXXXXYYWW) will change according to the time of production.



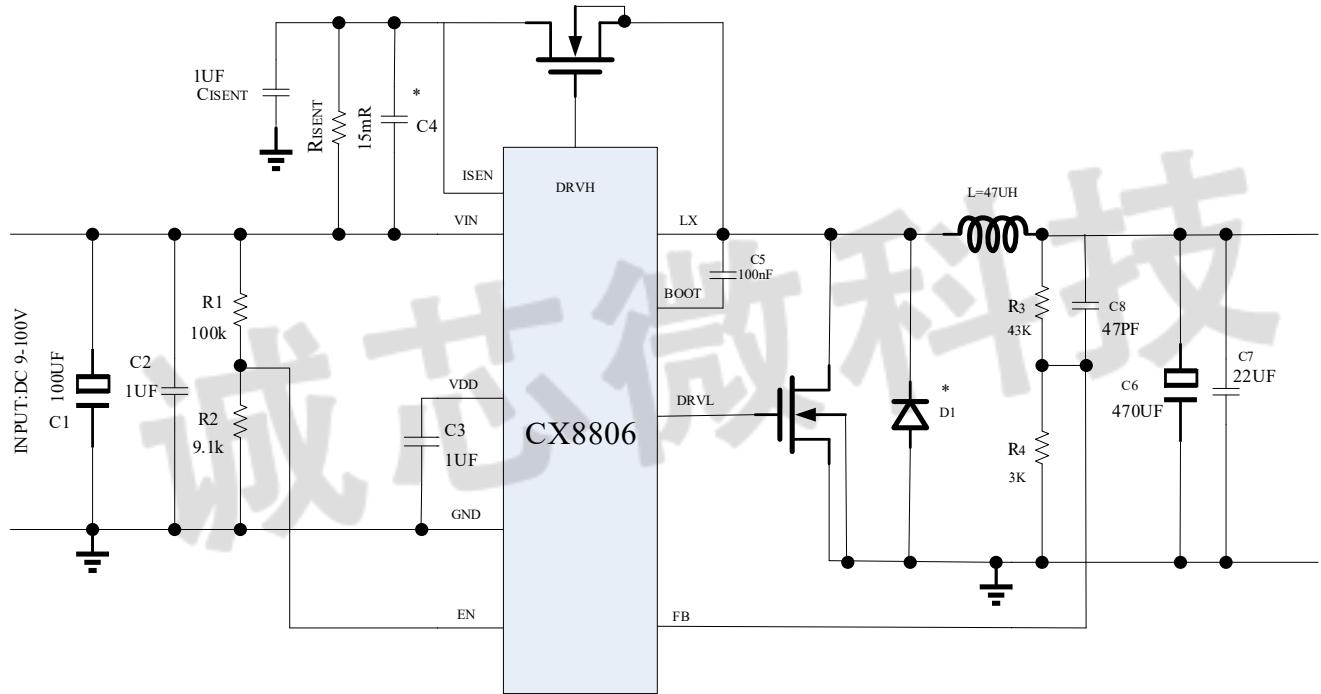
Pin Configuration



PIN	NAME	Description
1	ISEN	Connecting a resistance from ISEN to VIN sets the output short circuit detection threshold.
2	VIN	Input supply. VIN supplies power to all of the internal control circuitries, both BOOT regulators, and the high-side switch.
3	EN	Enable input. Pull EN below the specified threshold to shut down the. Pull EN above the specified threshold or leave EN floating to enable the .
4	GND	Ground. GND should be placed as close to the output capacitor as possible to avoid the high-current switch paths. Connect the exposed pad to GND plane for optimal thermal performance.
5	VDD	Power input to the controller.
6	FB	Feedback. FB is the input to the voltage hysteretic comparators. The average FB voltage is maintained at 800mV by loop regulation.
7	DRVL	Low Drive. Bootstrapped output for driving the gate of the low side N channel FET.
8	BOOT	Bootstrap. BOOT is the positive power supply for the internal, floating, high-side MOSFET driver. Connect a bypass capacitor between BOOT and SW.
9	SW	Switch node. SW is the output from the high-side switch. A low forward voltage Schottky rectifier to ground is required. The rectifier must be placed close to SW to reduce switching spikes.
10	DRVH	High Drive. Bootstrapped output for driving the gate of the high side N channel FET.

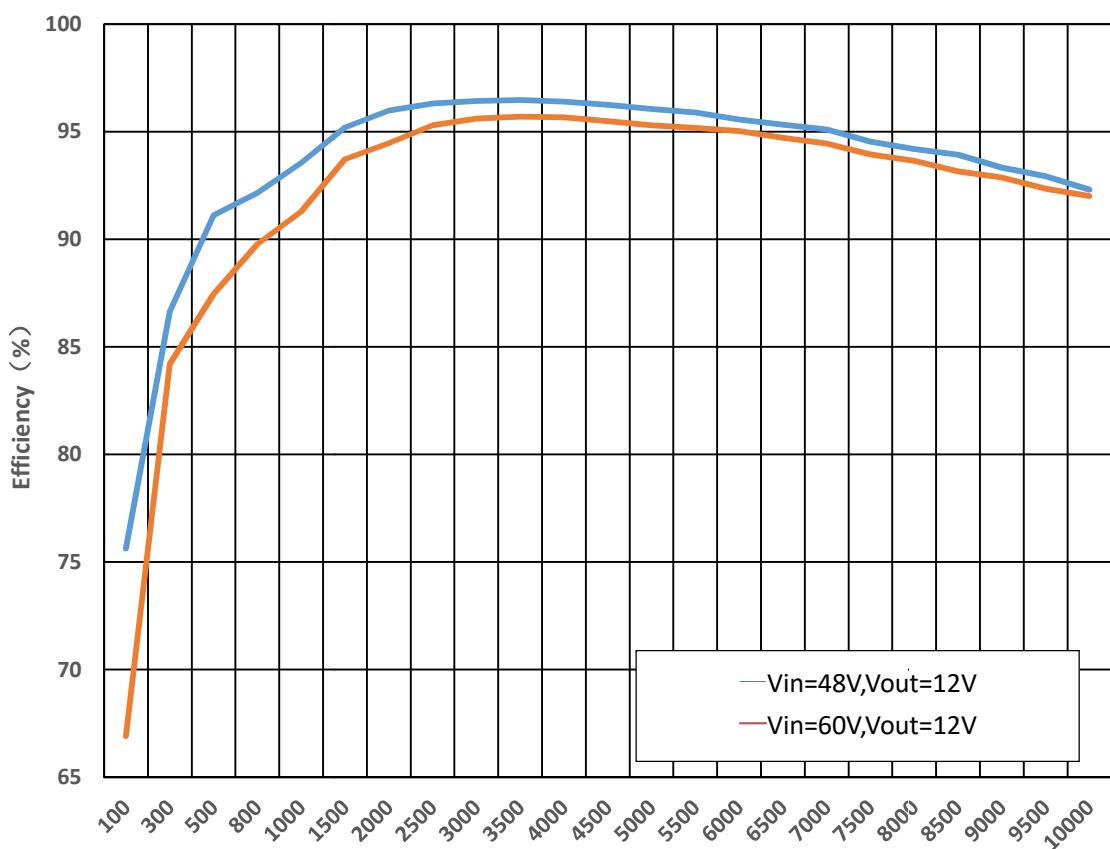


Typical Application



9V-100V, Synchronous Buck Converter

Efficiency





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Absolute Maximum Ratings

	Description	Min	Max	Unit
Input voltage	VIN to GND	-0.3	110	V
	EN to GND	-0.3	110	V
	FB to GND	-0.3	7	V
	ISEN to GND	-0.3	110	V
Output voltage	BOOT to GND	-0.3	110.5	V
	BOOT to SW	-0.3	5.5	V
	VDD to GND	-0.3	7	V
	SW to GND	-0.3	110	V
	DRVH to SW	-0.3	5.5	V
	DRVL to GND	-0.3	5.5	V
T _{stg}	Storage Junction Temperature	-55	150	°C
T _{solder}	Lead Temperature (Soldering 10 sec.)	260		°C

Note:

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

ESD Ratings

Item	Description	Range	Unit
V _{ESD}	Human Body Model(HBM)	2	KV
	Charged Device Model(CDM)	200	V

Note:

JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

JEDEC document JEP157 states that 200-V CDM allows safe manufacturing with a standard ESD control process.



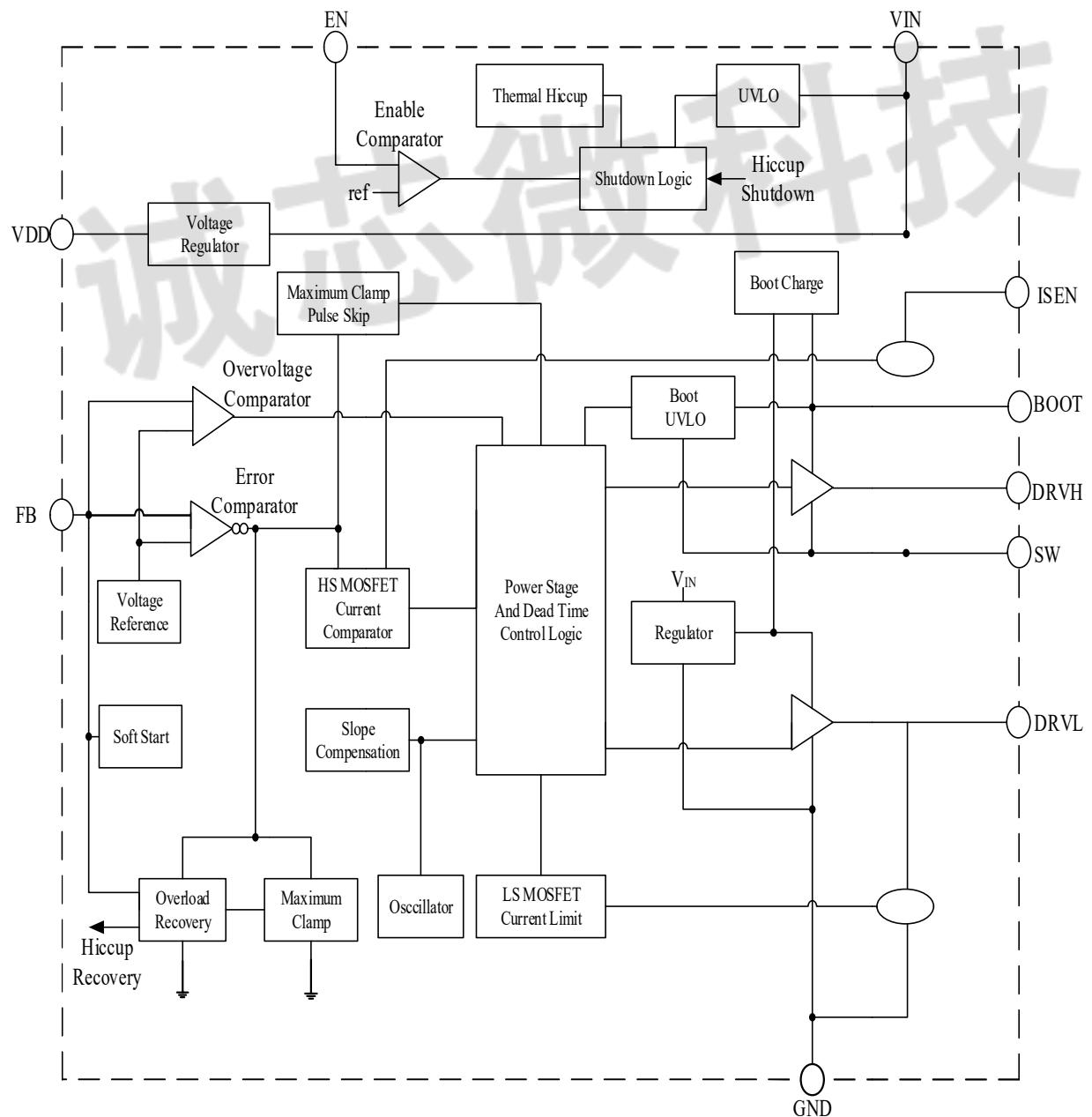
Electrical Characteristic

(At $T_A=25^\circ\text{C}$, $V_{IN}=48\text{V}$, $V_{OUT}=5\text{V}$, Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VCC SUPPLY VOLTAGE						
V_{IN}	Operating Input Voltage		9	-	100	V
V_{IN_UVLO}	Input UVLO Threshold	V_{IN} rising	-	8	-	V
$V_{UVLO(HY)}$	Input UVLO Hysteresis		-	0.3	-	V
I_{SHUT}	Shutdown supply current	$EN=0\text{V}$,no load	-	9	-	uA
I_Q	Quiescent Current from VIN pin	EN floating, no load, non-switching	-	500	-	uA
ENABLE						
V_{EN}	Enable threshold voltage		2.2	-	100	V
V_{EN_UVLO}	Enable threshold voltage Hysteresis		-	0.2	-	V
FEEDBACK						
V_{FB}	FB Reference Threshold		-	0.8	-	V
V_{FB} (short)	Feedback short voltage		-	0.35	-	V
V_{FB2}	Feedback short voltage Hysteresis		-	0.42	-	V
OSCILLATOR						
F_{SW}	Switching frequency	$I_{OUT}=500\text{mA}$	-	150	-	kHz
D_{MAX}	Maximum Duty Cycle	$V_{IN}=12\text{V}$	-	91	-	%
VDD						
VDD	VDD Voltage			5.4		V
CURRENT LIMIT						
V_{SEN}	Cycle-by-cycle sense voltage		-	150	-	mV
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown Temp		-	130	-	°C
T_{SH}	Thermal shutdown Temp Hysteresis		-	20	-	°C



Functional Block Diagram





pplications Information

Overview

The CX8806 is a high voltage, synchronous step-down controller operates over a wide range input voltage 9V to 100V. The CX8806 delivers 10A continuous load current with up to 96% efficiency. The CX8806 operates with fixed frequency peak current control with built-in compensation eliminates the need for external components. Cycle-by-cycle current limit in high-side MOSFET protects the converter in an overload condition. Hiccup mode protection is triggered if the over-current condition has persisted for longer than the present time. The CX8806 exhibits protection feature that protect the load from faults like under-voltage,over-current and over-temperature.

Over-current Protection:

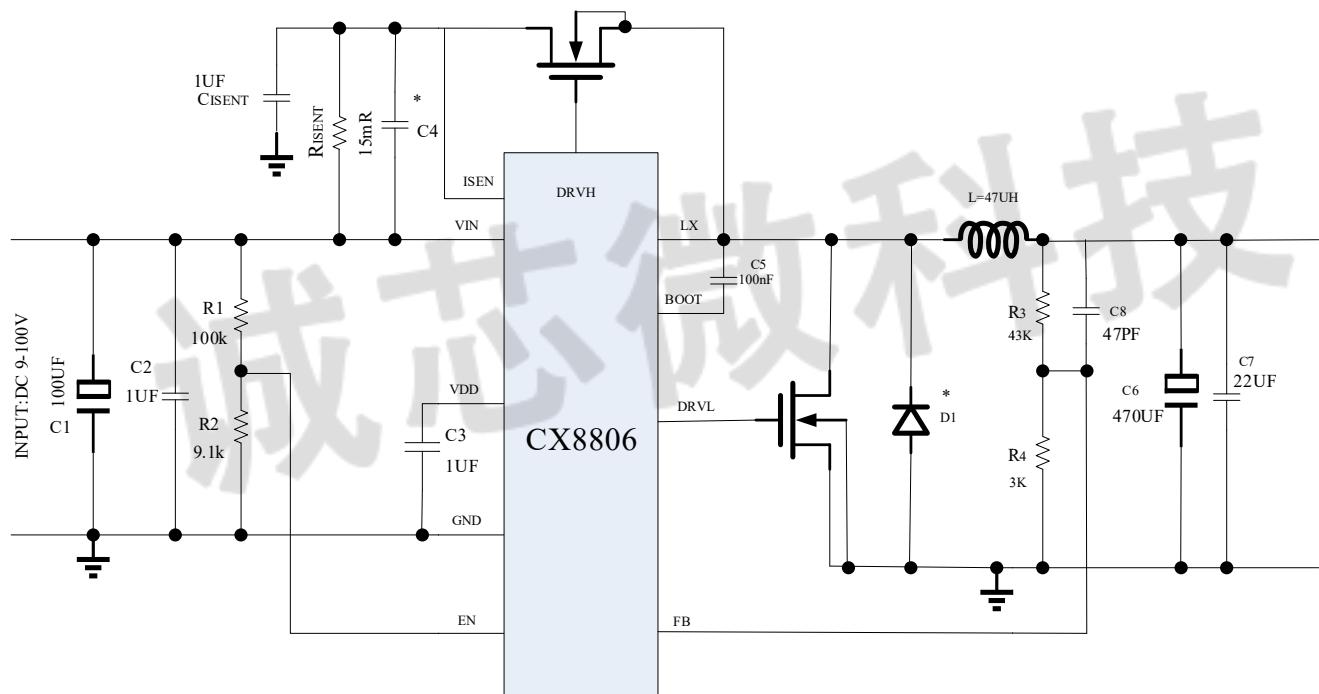
The CX8806 implements current-mode control which uses the internal COMP voltage to control the turn on and the turnoff of the high-side MOSFET on a cycle-by-cycle basis. During each cycle, the switch current and the current reference generated by the internal COMP voltage are compared.

Locking mode:

When $V_{FB} < V_{FB}$ (short) CX8806 enters a locked state, it needs to be re powered on after canceling the short circuit .



Typical Application



CX8806 Design Example, 12V Output with Programmable UVLO

Design Parameters	Example Value
Input Voltage	24V-100V
Output Voltage	12V
Maximum Output Current	5A
Switching Frequency	150Khz
Output voltage ripple (peak to peak)	75mV
Transient Response 1A to 3A load step	500mV
Start Input Voltage (rising VIN)	24V
Stop Input Voltage (falling VIN)	22V



Output Voltage

The output voltage is set by an external resistor divider R3 and R4 in typical application schematic. Recommended R4 resistance is 10KΩ. Use equation 1 to calculate R3.

$$R_3 = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) * R_4$$

Under Voltage Lock-Out

An external voltage divider network of R1 from the input to EN pin and R2 from EN pin to the ground can set the input voltage's Under Voltage Lock-Out (UVLO) threshold.

$$R_1 = \left(\frac{V_{UVLO}}{V_{EN}} - 1 \right) * R_2$$

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance(DCR).Larger inductance results in less inductor current ripple and theref-ore leads,

to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size,higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20%~40% of the maximum output current.

The peak-to-peak ripple current in the inductor ILPP can be calculated as in Equation:

$$I_{LPP} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{V_{IN} * L * f_{SW}}$$

ILPP is the inductor peak-to-peak current

L is the inductance of inductor

fSW is the switching frequency

VOUT is the output voltage

VIN is the input voltage

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation to calculate the inductance value

$$L_{MIN} = \frac{V_{OUT}}{f_{sw} * LIR * I_{OUT(max)}} * \left(1 - \frac{V_{OUT}}{V_{IN(max)}} \right)$$



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LMIN is the minimum inductance required

fsw is the switching frequency

VOUT is the output voltage

VIN(max) is the maximum input voltage

IOUT(max) is the maximum DC load current

LIR is coefficient of ILPP to IOUT

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, ILPEAK and ILRMS can be calculated as in equation :

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2}$$

$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{1}{12} * (I_{LPP})^2}$$

ILPEAK is the inductor peak current

IOUT is the DC load current

ILPP is the inductor peak-to-peak current

ILRMS is the inductor RMS current

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 1.5A.

The most conservative approach is to choose an inductor with a saturation current rating greater than 1.5A. Because of the maximum ILPEAK limited by device, the maximum output current that can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

Diode Selection

Requires an external catch diode between the SW pin and GND. The selected diode must have a reverse voltage rating equal to or greater than VIN(max). The peak current rating of the diode must be greater than the maximum inductor current. Schottky diodes are typically a good choice for the catch diode due to their low forward voltage. The lower the forward voltage of the diode, the higher the efficiency of the regulator. Typically, diodes with higher voltage and current ratings have higher forward voltages. A diode with a minimum of 100-V reverse voltage is preferred to allow input voltage transients up to the rated voltage of the CX8806.



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For the example design, the SS310 Schottky diode is selected for its lower forward voltage and good thermal characteristics compared to smaller devices. The typical forward voltage of the SS310 is 0.65 volts at 3 A.

The diode must also be selected with an appropriate power rating. The diode conducts the output current during the off-time of the internal power switch. The off – time of the internal switch is a function of the maximum input voltage, the output voltage, and the switching frequency. The output current during the off-time is multiplied by the forward voltage of the diode to calculate the instantaneous conduction losses of the diode. The ac losses of the diode need to be taken into account. The ac losses of the diode are due to the charging and discharging of the junction capacitance and reverse recovery charge. Equation 14 is used to calculate the total power dissipation, including conduction losses and ac losses of the diode.

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g. 1uF) with small package size (0805) to filter high frequency switching noise. Place the small size capacitor close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input

$$I_{CINRMS} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})}$$

The worst case condition occurs at $V_{IN}=2*V_{OUT}$, where:

$$I_{CINRMS} = 0.5 * I_{OUT}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 15 and the maximum input voltage ripple occurs at 50% duty cycle

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})$$



For this example, four 4.7 μ F, X7R ceramic capacitors rated for 60 V in parallel are used. And a 0.1 μ F for high-frequency filtering capacitor is placed as close as possible to the device pin

Bootstrap Capacitor Selection

A 0.1UF ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacito. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation desired.

$$\Delta V_{OUT} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * f_{SW}^2 * L * C_{OUT} * V_{IN}}$$

ΔV_{OUT} is the output voltage ripple

FSW is the switching frequency

L is the inductance of inductor

COUT is the output capacitance

VOUT is the output voltage

VIN is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, four 47F ceramic output capacitors work for most applications.



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Typical Characteristics

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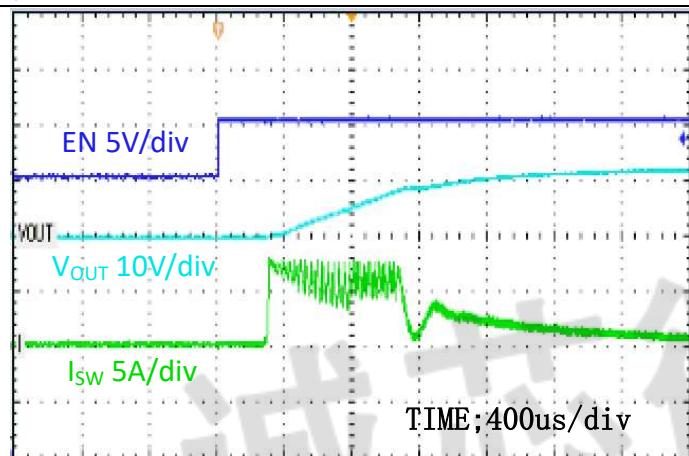


Figure1 EN Start up

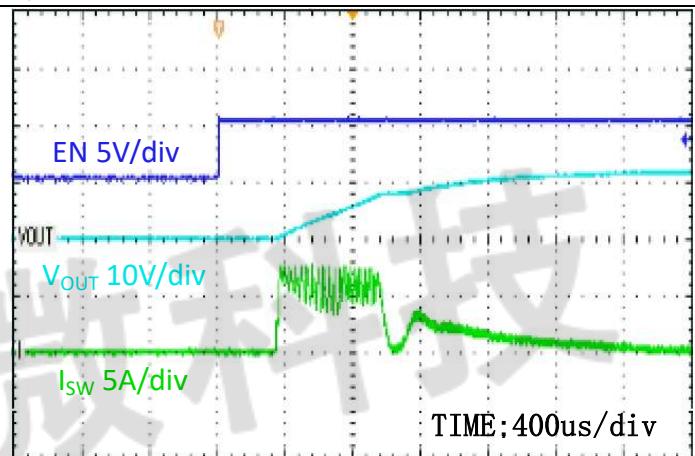
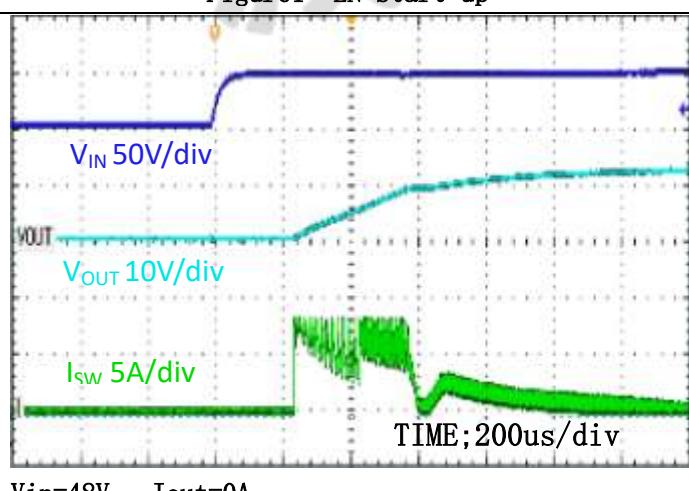


Figure2 EN Start up



Vin=48V

Figure3 Start up

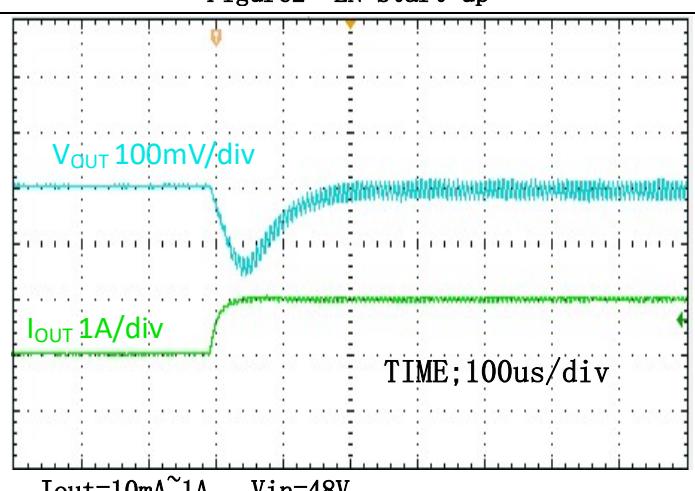
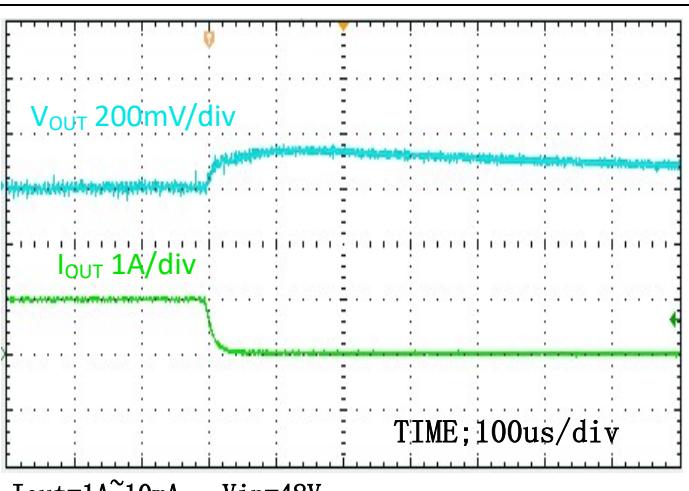


Figure4 Load Transient



Iout=1A~10mA

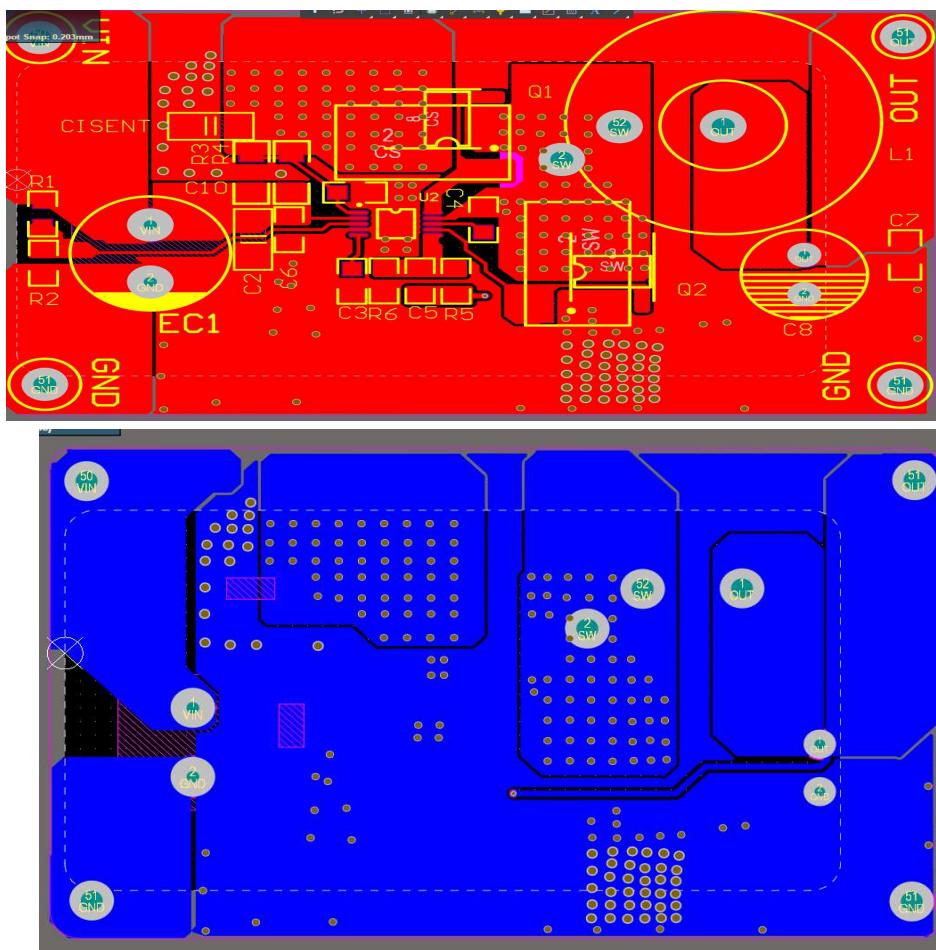
Figure5 Load Transient



LAYOUT

Proper PCB layout is a critical for CX8806's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impedance and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impedance of grounding.
4. Output inductor and low-side MOSFET should be placed close to the SW pin. The switching area of the PCB conductor minimized to prevent excessive cap active coupling.
5. Route BOOT capacitor trace on the other layer than top layer to provide wide path for topside ground.
6. Place a low ESR ceramic capacitor as close to VDD pin and the ground as possible to reduce parasitic effect.

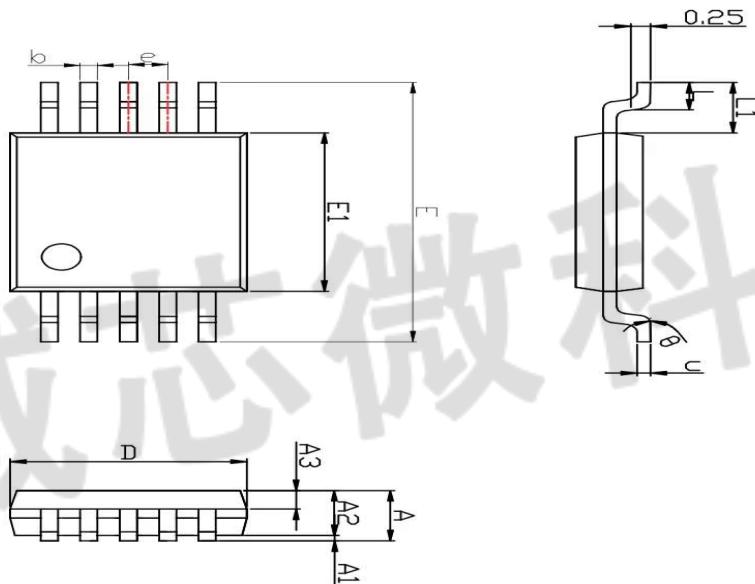




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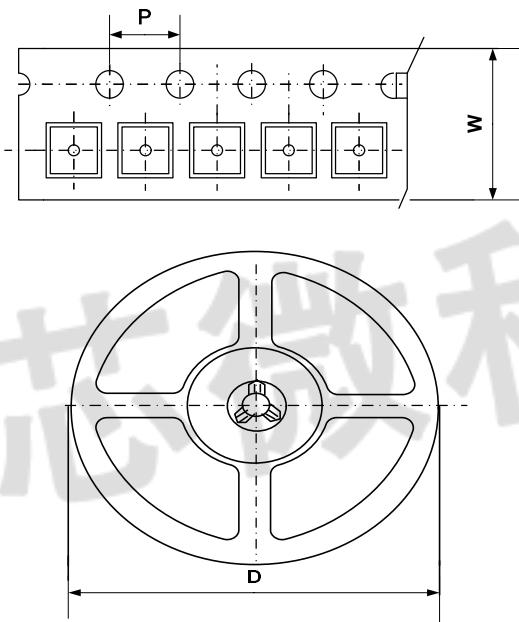
Package Outline



Symbol	Millimetre		
	Min	Typ	Max
A	—	—	1.10
A1	0.05	0.10	0.15
A2	0.80	0.85	0.90
A3	0.30	0.35	0.40
b	0.17	0.20	0.23
c	0.13	0.15	0.17
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.50BSC		
L	0.40	0.55	0.70
L1	0.90	0.95	1.00
θ	0°	—	8°



Packing Information



Type	W(mm)	D(mm)	Qty (pcs)
MSOP10	16.0±0.1 mm	330±1 mm	2500pcs

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